

Experiment No. 2

1. Title :

Architecture of Microprocessor 8086.

2. Prior Concepts :

- ALU, registers, bus, flags, memory pointers.
- Interrupt, clock, control and status signals.

3. New Concepts :

- Instruction queue, pipelining concept.
- Segment registers.

Proposition 1 :

Flag register:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	OF	DF	IF	TF	SF	ZF	x	AF	x	PF	x	CF

Proposition 2 :

Status of CPU following the RESET :

CPU	Contents	CPU	Contents
Flag register		Instruction pointer	
CS register	FFFFH	DS register	0000H
SS register		ES register	
Queue	Empty		

Complete the above table with appropriate information.

Proposition 3 :

Status bit definition :

S4	S3	Bus cycle access is to
0	0	
0	1	
1	0	Code segment register (or none)
1	1	

Complete the above table with appropriate information.

Proposition 4 :

Memory access encoding :

$\overline{\text{BHE}}$	A0	Action
0	0	
0	1	Access odd byte to D8 -D15
1	0	
1	1	No action

Complete the above table with appropriate information.

Proposition 5 :

Segment register assignment :

Type of memory reference	Default segment	Alternate segment	Offset (Logical address)
Instruction fetch	CS	None	IP
Stack operation	SS	None	SP
General data	DS	CS, ES, SS	Effective address
String source	DS	CS, ES, SS	SI
String destination	ES	None	DI
BX used as pointer	DS	CS, ES, SS	Effective address
BP used as pointer	SS	CS, ES, DS	Effective address

4. Learning Objectives :**Intellectual Skills:**

Understanding:

- a) Internal operations performed by microprocessor 8086.
- b) Use of internal resources of microprocessors 8086.

Motor Skills:

Drawing the block diagram and labeling it.

5. Theory:**Part A: theory**

- 8086 has 20-bit address bus, 16-bit data bus, three power supply pins and 17 pins for timing and control.
- 8086 requires a clock signal with fast rise and fall time (< 10 ns), and logic 0 level of $-0.5V$ to $0.6V$ and logic 1 level of $3.9V$ to $5.0V$ and duty cycle of 33 %.
- The processor's RESET signal must be synchronized to system clock and persist for at least $4T$ states.
- Internally 8086 microprocessor is designed with dynamic logic gates that require periodic refreshing. The clock signal provides this refreshing.

Part B:

Draw the block diagram of microprocessor 8086

Part C :

Write name of pins and major function of pins, as illustrated for pin number 17.

Pin No.	Name of pin	Function/s of pin in MIN mode	Function/s of pin in MAX mode (if applicable)
16 to 2 & 39			----
17	NMI	Non Maskable Interrupt	----
18			----
19			----
1, 20 & 40			----
21			----
22			----
23			----
24			
25			
26			
27			
28			
29			
30			
31			
32			----
33			----
34			----
38 to 35			----

6 Questions :

(Attempt four questions as directed by teacher.)

- 1) State the functions of EU and BIU.
- 2) Describe the address pipelining concept.
- 3) What is the maximum memory capacity of 8086 based system? Why?
- 4) Describe all the memory segments and segment registers.
- 5) State the relation between physical address & offset addresses.
- 6) What physical address is represented by following?
a) 4370:651DH b) 0000:0000H.
- 7) Which is first memory location accessed by CPU immediately after RESET? Why?
- 8) Why microprocessor 8086 is 16-bit CPU?
- 9) What is the maximum memory capacity of microprocessor 8086? Why?
- 10) State the conditions that set the different flags of microprocessor 8086.
- 11) State the purpose of the TF, DF and IF flags.
- 12) What are the contents of different registers immediately after RESET?
- 13) State requirements and functions of clock signal in microprocessor 8086.
- 14) State the default and alternate segments for the memory reference:
a) General data, b) Instruction fetch, c) Stack operation.

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