

**Course Name : Computer Engineering Group**

**Course Code : CO/CM/IF/CD**

**Semester : Third**

**Subject Title : Digital Techniques**

**Subject Code : 12064**

**Teaching and Examination Scheme:**

Teaching Scheme			Examination Scheme					
TH	TU	PR	PAPER HRS.	TH	PR	OR	TW	TOTAL
03	--	02	03	100	--	--	25@	125

**NOTE:**

- **Two tests each of 25 marks to be conducted as per the schedule given by MSBTE.**
- **Total of tests marks for all theory subjects are to be converted out of 50 and to be entered in mark sheet under the head Sessional Work. (SW)**

**Rationale:**

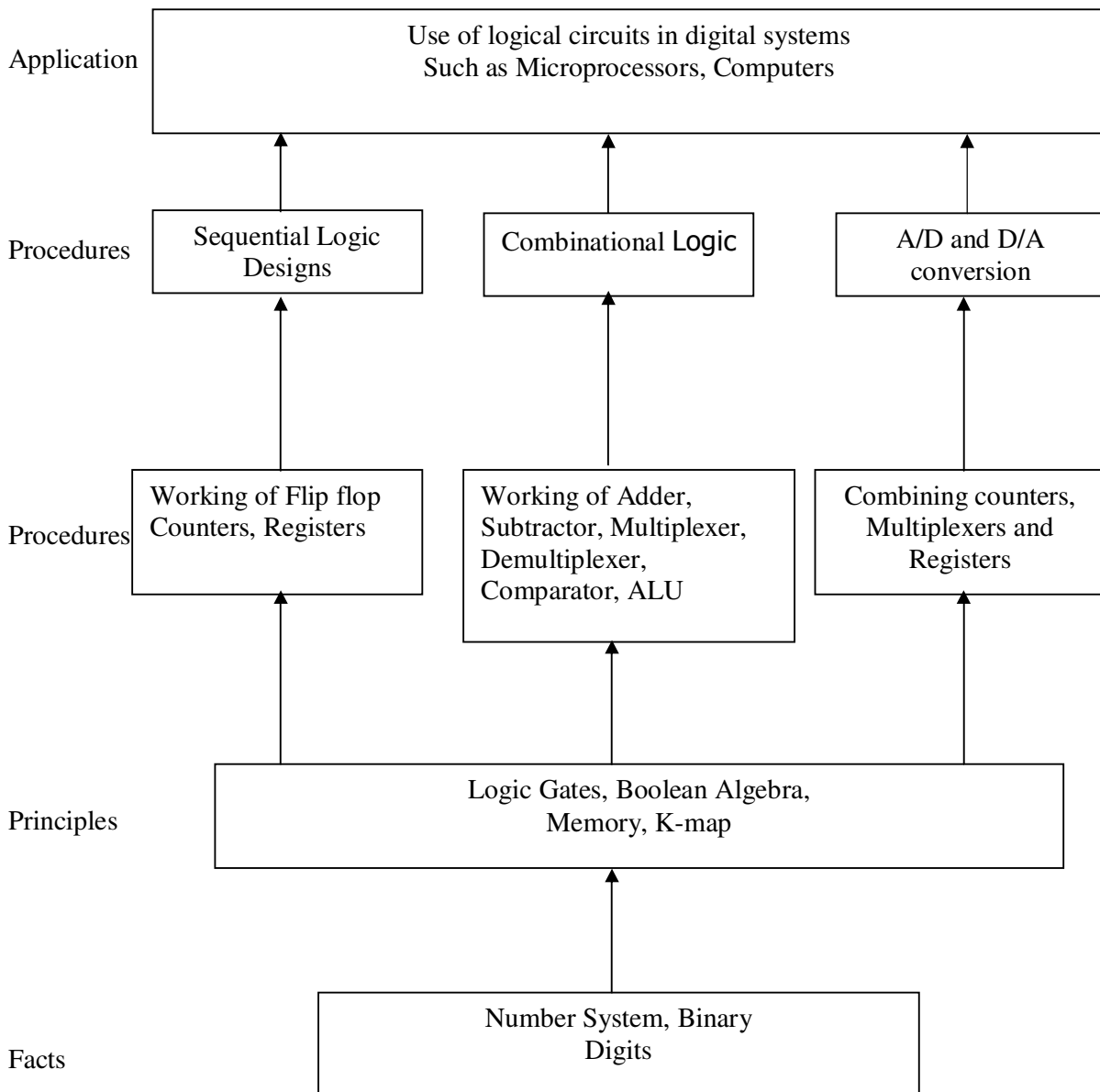
In the present era, applications of digital circuits are prevalent in consumer products right from calculators, digital diaries, digital watches, computers, mobile phones, to industrial products. So the digital technique has been introduced as a core technology subject in Computer Engineering curriculum. It will enable the students to assemble, design, test and troubleshoot logical circuits such as ALU, MUX, DEMUX, A/D and D/A converters. It deals with topics ranging from logic gates, to combinational and sequential logic circuits and memories. It lays a foundation for the knowledge of microprocessors and computers.

**Objectives:**

The student will be able to

1. Design simple logic circuits.
2. Assemble logic circuits.
3. Test the logic circuits.
4. Observe outputs of logic circuits.
5. Troubleshoot digital circuits.

**Learning structure:**



## Contents: Theory

Chapter	Contents	Hours	Marks
1	<b>Introduction To Digital Techniques</b>	08	16
	1.1 Digital circuit.		
	1.2 Digital signal.		
	1.3 Use of digital circuit and digital signal.		
	1.4 Advantages and Disadvantages of Digital circuits.		
	1.5 Generation of digital signal		
	1.6 Introduction to digital ICs, Characteristics of digital ICs		
	1.7 Logic families comparison of TTL, CMOS and ECL logic Families (No circuits) (To be covered in Practical)		
	1.8 Number System - Introduction to Binary, Octal, Decimal, Hexadecimal number system		
	1.9 Conversion of number systems		
	1.10 1's complement and 2's complement		
	1.11 Binary arithmetic (addition, subtraction).		
1.12 BCD code, BCD arithmetic (addition, subtraction).			
2	<b>Logic Gates And Boolean Algebra</b>	06	14
	2.1 Logical symbol, logical expression and truth table of AND, OR, NOT, NAND, NOR, EX-OR and EX-NOR gates.		
	2.2 Universal gates – NAND and NOR gates		
	2.3 Logical circuits of basic gates using universal gates		
	2.4 Gates using more than two inputs.		
	2.5 TTL and CMOS logic gate ICs and their pin configurations. (To be covered in Practical)		
	2.6 Basic laws of Boolean algebra, Duality theorem.		
2.7 De Morgan's theorems.			
3	<b>Combinational Logic Design / Circuits</b>	12	24
	3.1 Simplification of Boolean expression using Boolean algebra.		
	3.2 Construction of logical circuits forms Boolean expressions.		
	3.3 Boolean expressions using Sum of products and product of sums forms.		
	3.4 K-map representation of logical functions.		
	3.5 Minimization of logical expressions using K-map ( 2, 3, 4 variables).		
	3.6 Standardization of SOP & POS equations		
	3.7 Concept of Adders / Subtractors.		
	3.8 Truth table, K-map, Simplified logical expression and logical circuit using basic gates and universal gates of : (a) Half adder and full adder. (b) Half subtractor and full subtractor.		
	3.9 Block diagram, Truth table, Logical expression and logic diagram of Multiplexers (4:1 and 8:1), Multiplexer IC.		
	3.10 Block diagram and Truth table of Demultiplexer (1:4; 1:8; 1:16), Demultiplexer IC.		
	3.11 Block diagram and Truth table of Encoders, Priority Encoders ICs and Decoder.		
3.12 Block diagram, Truth table, working principle, Applications, pin functions of Decimal to BCD Encoder (IC 74147) and BCD to 7-segment Decoder.			
Block diagram and function table of Parity generator (IC 74180),			

	Digital comparator IC (7485); Block diagram and pin functions of ALU 74181		
<b>4</b>	<b>Flip Flops And Sequential Logic Design</b> 4.1 One-bit memory cell, clock signal 4.2 Symbol and Logic diagram using NAND gates, working and truth table of R S flip-flop. 4.3 Symbol and Logic diagram using NAND gates, working, truth table and timing diagram of Clocked R S flip flop. 4.4 Triggering: edge triggering and level triggering 4.5 Symbol and Logic diagram using NAND gates, working, truth table and timing diagram of J-K flip flop. 4.6 Block diagram and truth table of Master slave J-K flip flop. 4.7 Symbol, working and truth table of D- flip flop and T-flip flop. 4.8 Applications of flip flops 4.9 Concept, Modulus, Working, truth table, timing diagram of a counter. 4.10 Asynchronous counter (3 bit, 4 bit); 4.11 Design of mod N-counter: working, truth table and timing diagram 4.12 3-bit Synchronous counter: working, truth table and timing diagram 4.13 Block diagram, Working, Truth Table and waveforms of Shift register: SISO, SIPO, PISO, PIPO (4-bit) and Universal Shift register (4-bit). 4.14 Applications of Counters and Registers.	12	24
<b>5</b>	<b>Memories</b> 5.1 Classification of memories 5.2 RAM, ROM, PROM, EPROM, E <sup>2</sup> PROM. 5.3 Circuit diagram using CMOS transistors and working of Static and dynamic RAM	04	08
<b>6</b>	<b>A-D And D-A Converters</b> 6.1 Circuit diagram and working of R-2R Ladder DAC and Weighted resistor DAC. 6.2 DAC specifications 6.3 Block diagram and working of Ramp ADC, Dual slope ADC and Successive approximation ADC. 6.4 ADC specification 6.5 Advantages and Disadvantages of various methods.	06	14
<b>Total</b>		<b>48</b>	<b>100</b>

**Practical:**

Skills to be developed:

Intellectual Skills:

1. Interpret the results
2. Verify the tables

**List of Practical: (Any TEN) including MINI PROJECT**

- 1) Study of Digital IC datasheets and noting down the characteristics for TTL & CMOS logic families.

- 2) Verification of truth table of logic gates.
- 3) Verification of De Morgan's theorem.
- 4) Construction of Half adder and Full adder.
- 5) Implementation of Combinational Circuit using Multiplexer.
- 6) Construction of 7-segment decoder driver.
- 7) Verification of truth table of Flip flops.
- 8) Universal Shift Register
- 9) Decade counter using IC 7490.
- 10) Design of 3-bit Synchronous counter.
- 11) A to D Converter.
- 12) Study of data sheets related to digital ICs like \_\_\_\_\_.
- 13) A MINI PROJECT (Design, Assemble, Test and Troubleshoot) integrating minimum two digital ICs.

Learning Resources:

**Books:**

Sr. No.	Author	Title	Publisher
01	R.P. Jain	Modern Digital Electronics	Tata McGraw Hill
02	Malvino Leach	Digital Principles	Tata McGraw Hill
03	Tokheim	Digital Electronics	Tata McGraw Hill
04	S.P. Bali	2000 solved problems in Digital Electronics – Sigma series	Tata McGraw Hill