

Course Name : Digital Electronics

Course Code: DE

Semester : Fourth

Subject Title : Digital System Design

Subject Code: 9075

Teaching and Examination Scheme:

Teaching Scheme			Examination Scheme						
TH	TU	PR	PAPER HRS	TH	TEST	PR	OR	TW	TOTAL
03	--	02	03	80	20	--	25#	25@	150

Rationale:

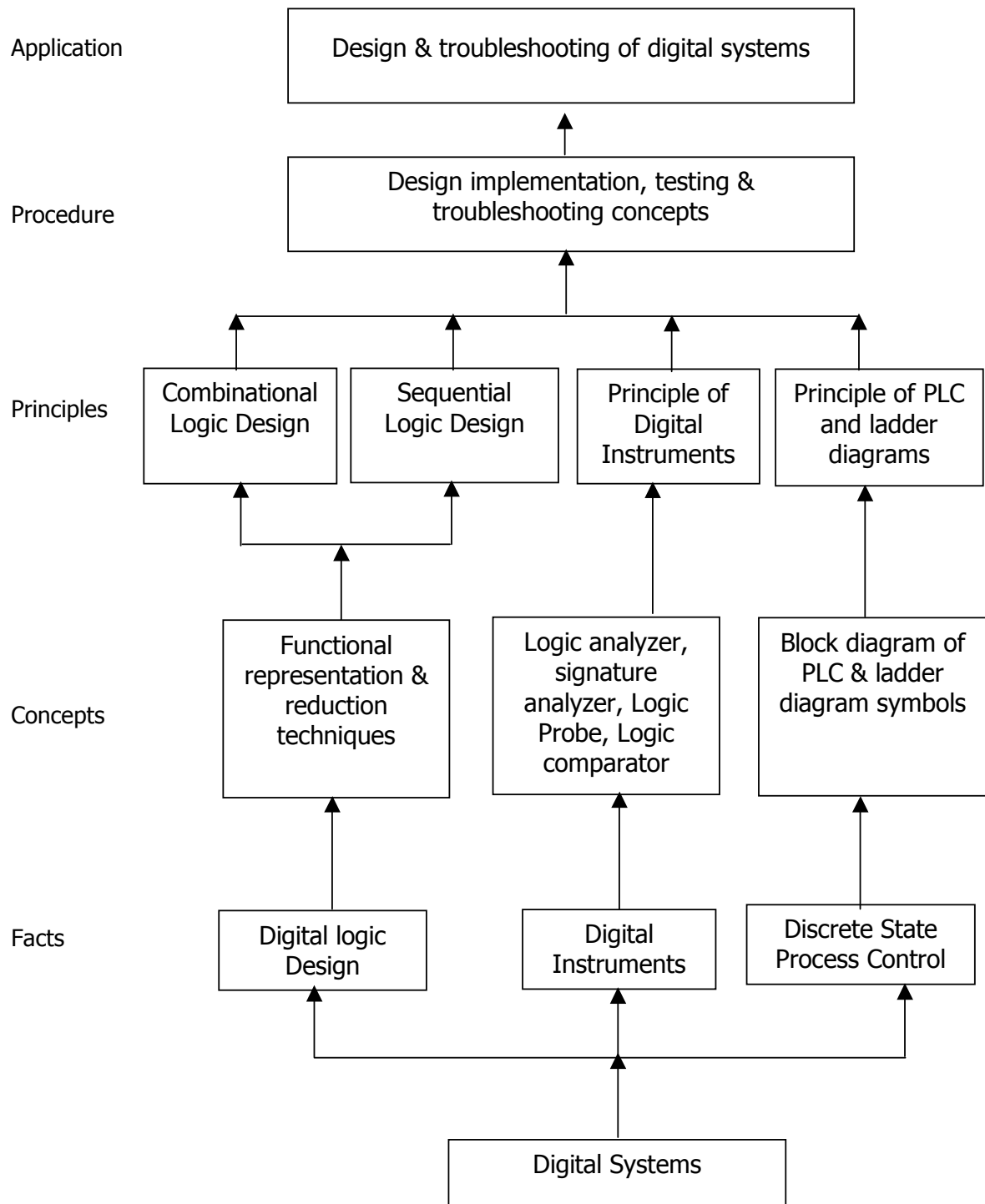
The engineers and technicians are expected to have thorough knowledge of Digital System Design and trouble shooting of digital systems. This course enables the students to learn design concepts by Quine-Mccluskey method, state diagrams and Moore-Mealy machines. Concepts of hazards in digital system will enable the student to troubleshoot digital circuits. The applications of logic circuits are covered by programmable logic circuits.

Objectives:

The students will be able to:

1. Design and analyze combinational circuits.
2. Do conversion of flip-flops.
3. Design and analyze sequential circuits.
4. Develop basic logic functions using PLC and basic ladder diagram for digital control applications.
5. Troubleshoot digital circuits using various troubleshooting equipments.

Learning Structure:



Contents: Theory

Chapter	Name of the Topic	Hours	Marks
01	Combinational Logic Design 1.1 Review of SOP & POS (min term & Max term) - K-Map for 5 & 6 variables, Quine- Mc cluskey method, Veitch Diagram, Map entered variable method. 1.2 Multiple output (2 level) NAND & NOR network. 1.3 4 bit binary multiplier, Binary divider. 1.4 Comparators – one bit, two bit & n bit comparators. IC – 7485, Parity checker & generator IC – 74180.	12	20
02	Flip – flop Design 2.1 Review of Excitation Table of SR, JK, D & T flip flop, Clocked SR flip flop design using NAND latch & its characteristic equation. 2.2 Conversion of one type of flip flop to another flip flop. 2.3 Flip-flop timing specifications – clock parameter, pulse width & skew, setup, Hold and delay time metastability.	08	14
03	Introduction to Sequential Circuits 3.1 Need, General model of sequential or FSM. 3.2 Mealy and Moore models - State machine notations – Input / output variable, excitation variable, Present state, Next state, State Table, Transition Table, State Diagram, Moore and Mealy model of flip-flops. 3.3 Designing steps for synchronous sequential circuits, Examples based on synchronous sequential circuits, 2 bit up down counter, sequence generator, serial adders etc. 3.4 Asynchronous sequential machines, Need & features of asynchronous FSM.	14	20

04	<p>Programmable Logic Devices & Controllers</p> <p>4.1 Programmable Read only Memory, Programmable Logic Array, Programmable Array Logic (PAL).</p> <p>4.2 Realization of sequential circuits using PLD's.</p> <p>4.3 Characteristics of programmable logic controller, Block diagram of PLC, Principle of operation, Symbols and Ladder Diagram for AND, OR, NOT logic function.</p>	08	14
05	<p>Testing & Troubleshooting of Digital Systems</p> <p>5.1 Combinational logic Hazards – static & dynamic, detection of static 0 & 1 Hazards, Problems due to clock & clock signals, noise and asynchronous input, Handshaking problem, Hang up state.</p> <p>5.2 Troubleshooting equipments: Logic Analyzer, Signature Analyzer, Logic Probe, and Logic Comparator.</p>	06	12
Total		48	80

Practical:

Skills to be developed:

Intellectual Skills:

1. Classification of different digital circuits for required application.
2. Ability to design the digital circuit & interpret the data located using data manuals related to experiments in lab.

Motor Skills:

1. Ability to build the circuit.
2. Observe the result and compare with the aim of experiment.
3. Handling the digital instruments.

List of Practical:

1. Verify operation of 4 bit magnitude comparator IC – 7485.
2. Verify operation of Parity Generator / Checker IC – 74180.
3. Design & verify the conversion of JK F/F into D & T using IC 7476 & basic gates.

4. Design & implement serial adder using shift registers & D flip flop.
5. Design & implement 2 bit up-down counter and draw state diagram (use IC- 7476).
6. Design a sequential network to convert BCD to excess – 3 code. The input and output will be serial with least significant bit first.
7. Design a mod – 7 asynchronous counter using IC 7476.
8. Design mod-4 synchronous counter using IC 7476.
9. Prepare the ladder diagram for any suitable application available in your lab.
10. Prepare a ladder diagram to switch ON and OFF a D.C. Motor.
11. Observe the instruction cycle of microprocessor or clock cycles available in your lab & measure the time duration using logic analyzer (4 hrs. to be allotted for this practical).

Mini Projects: (ANY ONE)

1. Design a mealy sequential network which investigates an input sequence 'X' and which will produce an O/P of Z=1 for any input sequence ending in 1010 provided that the sequence 001 has occurred at least once Eg. – X =10100101010, Z = 00000000101
2. Design a serial subtractor with accumulator for 4 bit binary numbers. Assume that negative numbers are represented by 2's complement.
3. Design 24 bit magnitude comparator using IC 7485.
4. Design $F1 = f(A,B,C) = \sum m_i(0,2,5,7)$, $F2 = f(A,B,C) = \sum m_i(3,6,7)$ using AND – OR logic/ PLA.

Learning Resources:

Books:

Sr. No.	Author	Title	Publisher
01	Charles H. Roth	Fundamentals of Logic Design	Jaico
02	M. Morris Mano	Digital Logic and Computer Design	Prentice Hall India
03	Gray Dunning	Introduction to Programmable Logic Controller	Thomson
04	R.P. Jain	Modern Digital Electronics	Tata McGraw Hill
05	John M. Yarbrough	Digital Logic Application and Design	Thomson
06	William I. Fletcher	An Engineering Approach to Digital Design	Prentice Hall India
07	Richard F. Tinder	Engineering Digital Design	Harcourt India
08	Douglas M. Considine	Process / Industrial Instruments and Controls Handbook	McGraw Hill
09	S. R. Bhutiyani	Advance Digital Techniques & Digital System Design	Everest Publishing House, Pune